



# QD2050 series High-voltage High-current Darlington Transistor Arrays

## Features

- 500-mA-Rated Collector Current(single output)
- High-Voltage Outputs: 50V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

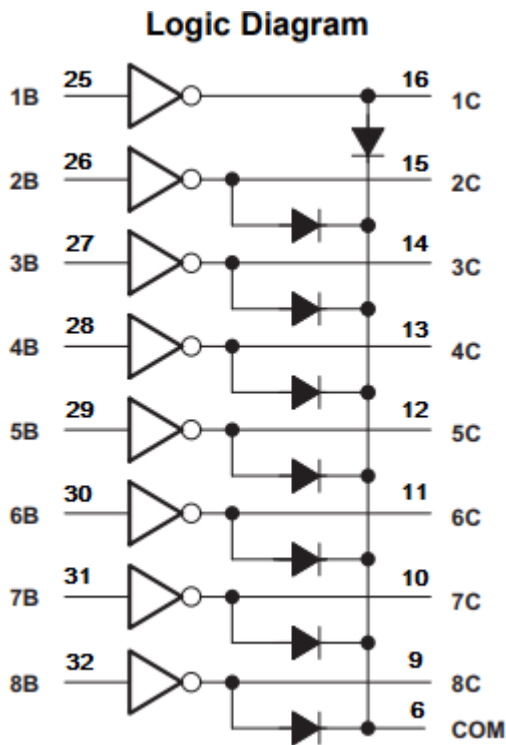
## General Description

The QD2050 is high-voltage high-current Darlington transistor arrays each containing eight open collector common emitter pairs. Each pair is rated at 500mA. Suppression diodes are included for inductive load driving, the inputs and outputs are pinned in opposition to simplify board layout.

These devices are capable of driving a wide range of loads including solenoids, relays, DC motors, LED displays, filament lamps, thermal print-heads and high-power buffers.

The QD2050 is available in both a small outline QFN-5\*5-32L package.

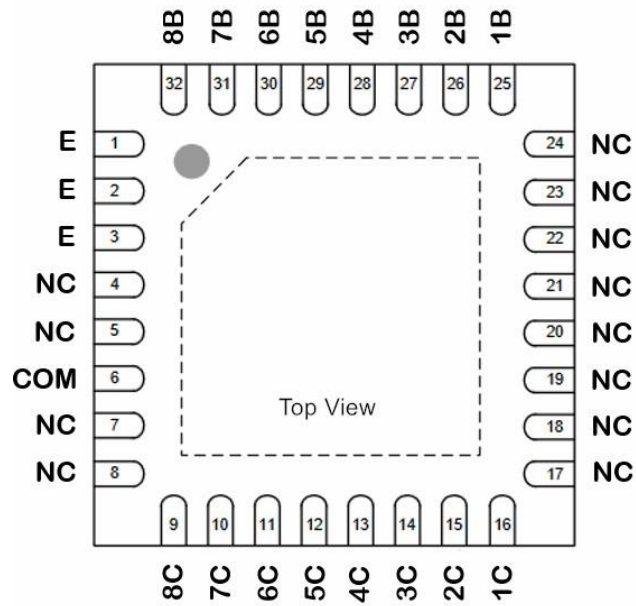
## Connection Diagram





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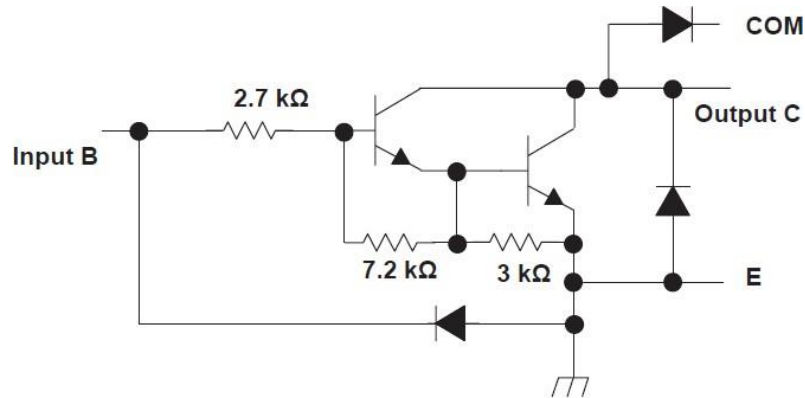
### Pin Descriptions



Pin Number	Pin Name	Function	Pin Number	Pin Name	Function
1	E	Common Emitter (ground)	17	NC	NC
2	E	Common Emitter (ground)	18	NC	NC
3	E	Common Emitter (ground)	19	NC	NC
4	NC	NC	20	NC	NC
5	NC	NC	21	NC	NC
6	COM	Common Clamp Diodes	22	NC	NC
7	NC	NC	23	NC	NC
8	NC	NC	24	NC	NC
9	8C	Output pair8	25	1B	Input pair1
10	7C	Output pair7	26	2B	Input pair2
11	6C	Output pair6	27	3B	Input pair3
12	5C	Output pair5	28	4B	Input pair4
13	4C	Output pair4	29	5B	Input pair5
14	3C	Output pair3	30	6B	Input pair6
15	2C	Output pair2	31	7B	Input pair7
16	1C	Output pair1	32	8B	Input pair8



## Functional Block Diagram



Note: All resistor values shown are nominal.

The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

## Absolute Maximum Ratings <sup>(1)</sup>

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Collector to emitter voltage	--	50	V
V <sub>R</sub>	Clamp diode reverse voltage <sup>(2)</sup>	--	50	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	--	30	V
I <sub>CP</sub>	Peak collector current	--	500	mA
I <sub>OK</sub>	Output clamp current	--	500	mA
I <sub>TE</sub>	Total emitter-terminal current	--	-2.5	A
T <sub>A</sub>	Operating free-air temperature range	-30	+105	°C
θ <sub>JA</sub>	Thermal Resistance Junction-to-Ambient <sup>(3)</sup>	--	63	°C/W
θ <sub>JC</sub>	Thermal Resistance Junction-to-Case <sup>(4)</sup>	--	12	
T <sub>J</sub>	Operating virtual junction temperature	--	150	°C
T <sub>STG</sub>	Storage temperature range	-40	150	°C

Note:

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of T<sub>J</sub> (max), θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) - T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of T<sub>J</sub>(max), θ<sub>JC</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) - T<sub>A</sub>)/θ<sub>JC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Collector to Emitter voltage	--	50	V
T <sub>A</sub>	Operating Ambient Temperature	-30	+105	°C



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### Electrical Characteristics (TA = +25°C, unless otherwise specified)

Symbol	Parameter	Test Figure	Test Conditions		MIN	TYP	MAX	Unit
V <sub>I(ON)</sub>	On-state input voltage	Figure 6	V <sub>CE</sub> = 2 V	I <sub>C</sub> = 200 mA	--	--	2.4	V
				I <sub>C</sub> = 250 mA	--	--	2.7	
				I <sub>C</sub> = 300 mA	--	--	3	
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	Figure 5	I <sub>I</sub> = 250 μA, I <sub>C</sub> = 100 mA	--	0.9	1.1	V	
			I <sub>I</sub> = 350 μA, I <sub>C</sub> = 200 mA	--	1	1.3		
			I <sub>I</sub> = 500 μA, I <sub>C</sub> = 350 mA	--	1.2	1.6		
I <sub>CEX</sub>	Collector cutoff current	Figure 1	V <sub>CE</sub> = 50 V, I <sub>I</sub> = 0	--	--	50	μA	
		Figure 2	V <sub>CE</sub> = 50 V, T <sub>A</sub> = +105°C, I <sub>I</sub> = 0	--	--	100		
V <sub>F</sub>	Clamp forward voltage	Figure 8	I <sub>F</sub> = 350 mA		--	1.7	2	V
I <sub>I(off)</sub>	Off-state input current	Figure 3	V <sub>CE</sub> = 50 V, I <sub>C</sub> = 500 μA		50	65	--	μA
I <sub>I</sub>	Input current	Figure 4	V <sub>I</sub> = 3.85 V		--	0.93	1.35	mA
			V <sub>I</sub> = 5 V		--	--	--	
			V <sub>I</sub> = 12 V		--	--	--	
I <sub>R</sub>	Clamp reverse current	Figure 7	V <sub>R</sub> = 50 V	--	--	--	50	μA
				T <sub>A</sub> = 70°C	--	--	100	
C <sub>i</sub>	Input capacitance	--	V <sub>I</sub> = 0, f = 1 MHz		--	15	25	pF

### Switching Characteristics (TA = +25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	(Figure 9)	--	0.25	1	μs
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	(Figure 9)	--	0.25	1	μs
V <sub>OH</sub>	High-level output voltage after switching	V <sub>S</sub> = 50 V, I <sub>O</sub> = 300 mA, (Figure 9)	V <sub>S</sub> -20	--	--	mV

**Parameter Measurement Information**

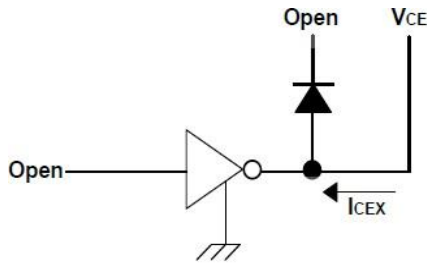


Fig.1 ICEX Test Circuit

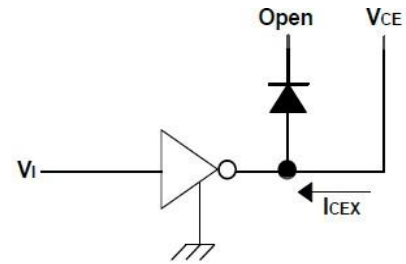


Fig.2 ICEX Test Circuit

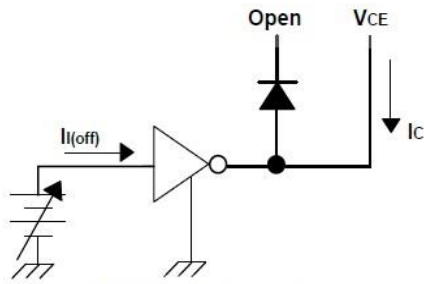


Fig.3 I(off) Test Circuit

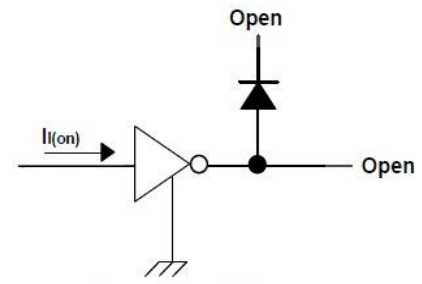


Fig.4 I(on) Test Circuit

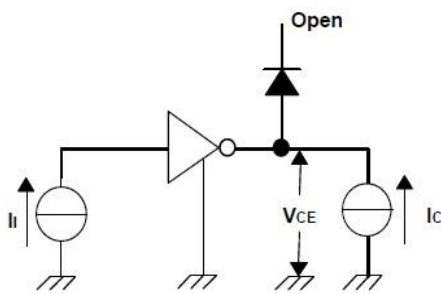


Fig. 5  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit

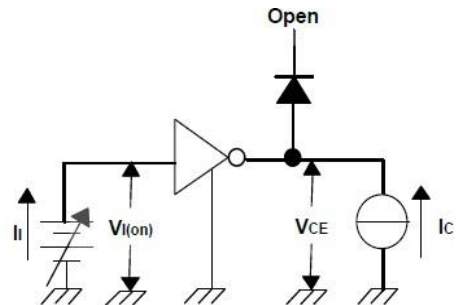


Fig. 6  $V_{I(on)}$  Test Circuit

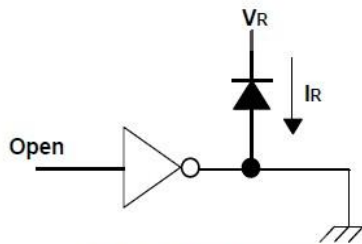


Fig. 7  $I_R$  Test Circuit

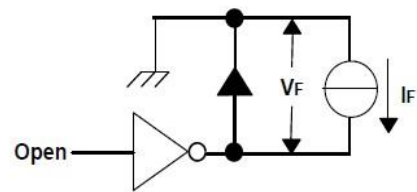


Fig. 8  $V_F$  Test Circuit

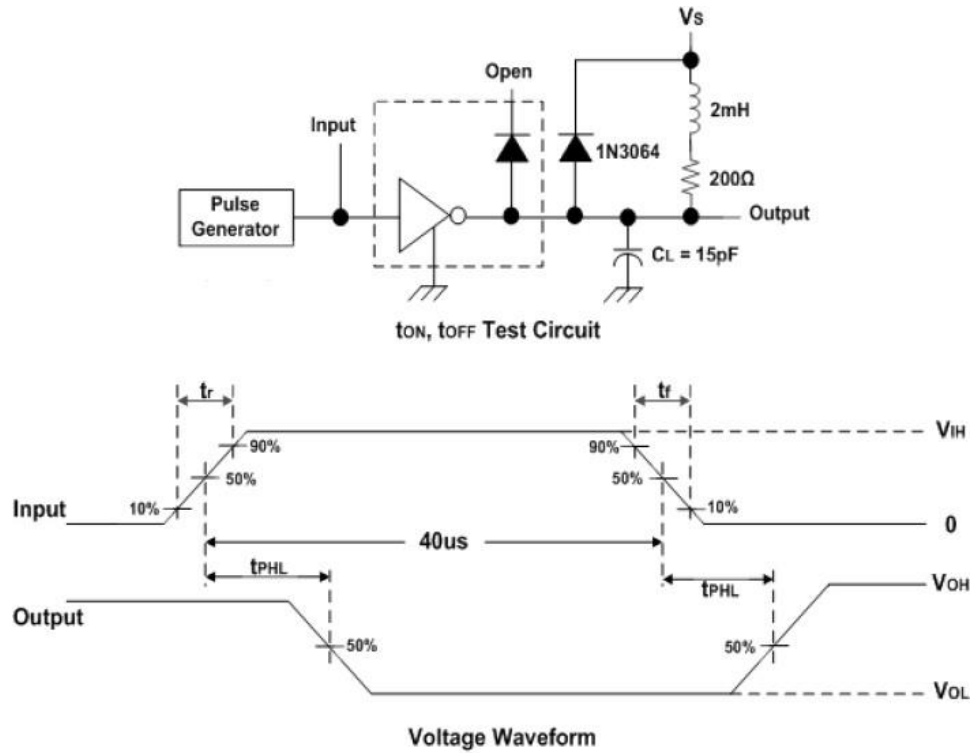
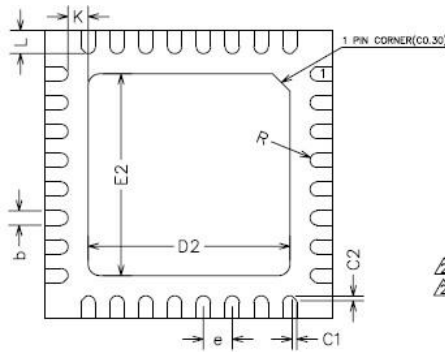
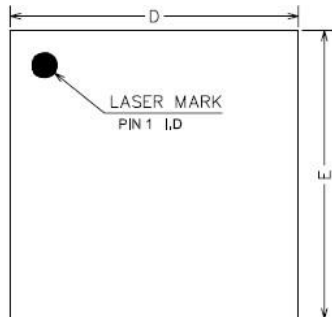


Fig. 9 Latch-Up Test Circuit and Voltage Waveform



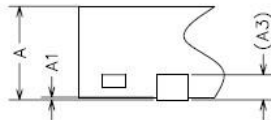
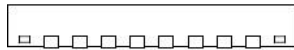
## QD2050 series High-voltage High-current Darlington Transistor Arrays

### QFN32 Outline Dimensions



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20REF		
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	-	-
L	0.35	0.40	0.45
R	0.09	-	-
C1	-	0.08	-
C2	-	0.08	-



NOTES:  
ALL DIMENSIONS REFER TO JEDEC STANDARD  
MO-220 WHHD-4.



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